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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,755	11/12/2003	Sung-Min Kim	5649-1147	7540
7590	03/02/2005		EXAMINER	
Robert N. Crouse Myers Bigel Sibley & Sajovec, P.A. P.O. Box 37428 Raleigh, NC 27627			SMOOT, STEPHEN W	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/706,755	KIM ET AL.
	Examiner	Art Unit
	Stephen W. Smoot	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 November 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-21 is/are pending in the application.
 4a) Of the above claim(s) 9-21 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-3 and 5-7 is/are rejected.
 7) Claim(s) 4 and 8 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 12 November 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 12 November 2003.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-8 are drawn to an integrated circuit structure, classified in class 257, subclass 347.
 - II. Claims 9-21 are drawn to a method of forming an integrated circuit structure, classified in class 438, subclass 149.
2. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another

and materially different process such as a process that does not include the applicant's as-claimed replacing step of a silicon layer with an insulation layer.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.
4. During a telephone conversation with Robert N. Crouse on 07 February 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-8. Affirmation of this election must be made by applicant in replying to this Office action. Claims 9-21 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.
5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Integrated Circuit Structure Including an Epitaxial Silicon Layer that Extends from an Active Region Through an Insulation Layer to an Underlying Substrate.

7. The disclosure is objected to because of the following informality:

On page 6, line 8, change "10" to --12-- because the sacrificial layer has been designated as reference character 12 (see page 5, line 17).

Appropriate correction is required.

Claim Objections

8. Claim 2 is objected to because of the following informality:

In claim 2, line 3, change "though" to --through-- to correct spelling.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-2, 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (US 2002/047158 A1).

Referring to Fig. 9 and paragraphs [0026] to [0037], Park et al. disclose an SOI MOSFET with the following structural features:

- A semiconductor substrate (50);
- A buried oxide layer (51) on the semiconductor substrate (50);
- A silicon channel region (440) separated from peripheral silicon active regions (49) by isolation regions (41) formed on the buried oxide layer (51);
- A body contact (444, 446) formed through the buried oxide layer (51) to electrically connect the silicon channel region (440) to an impurity doped ohmic region (60) of the semiconductor substrate (50); and
- The body contact (444, 446) can be formed from epitaxial silicon (see paragraph [0037]).

These are all of the limitations set forth in claims 1, 5 of the applicant's invention.

Regarding claims 2, 6, the above structure disclosed by Park et al. appears to be substantially identical to the applicant's structure implied by the as-claimed thermal oxidation process. Accordingly, per MPEP section 2113, a *prima facie* case of anticipation has been established and the burden now shifts to the applicant to show that the structures are not the same.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 2002/047158 A1) as applied to claim 2 above, and further in view of Hong (US 2002/0093041 A1).

As shown above, Park et al. anticipate claim 2 of the applicant's invention. However, Park et al. lack a nitride liner layer formed in the trench between two oxide layers, which is a further limitation to claim 2 that is set forth in claim 3 of the applicant's invention. Referring to Fig. 1 and paragraphs [0024] to [0028], Hong teaches a trench isolation region (20) that includes an anti-oxidative liner (50), which can be silicon nitride, formed between two oxide layers (40, 60).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the isolation regions of Park et al. by including the silicon nitride liner layer formed between two oxide layers as taught by Hong. Hong recognizes that the nitride liner layer is effective at preventing erosion of the isolation region during subsequent wet etching steps (see paragraph [0027]).

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US 2002/047158 A1) as applied to claim 1 above, and further in view of Spratt et al. (US 4,982,263).

As shown above, Park et al. anticipate claim 1 of the applicant's invention. However, Park et al. lack a strained silicon crystalline structure, which is the further limitation to claim 1 that is set forth in claim 7 of the applicant's invention. Referring to Figs. 2-7 and column 3, line 42 to column 6, line 52, Spratt et al. disclose a strained silicon structure that includes a silicon-germanium sublayer (32) formed between a silicon substrate and an SOI layer (34), which is subsequently anodized and oxidized to convert it into an isolation layer as shown in Fig. 5.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Park et al. and Spratt et al. in order to form a strained silicon structure as taught by Spratt et al. Spratt et al. recognize that the resulting SOI structure effectively maintains a uniform impurity concentration (see column 6, lines 28-37).

Allowable Subject Matter

14. Claims 4, 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

- Claim 4 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit structure that includes a trench isolation structure with a nitride liner formed between a thermal oxide layer and a field oxide layer, wherein the nitride liner extends into an insulation layer that is formed beneath an active region of an integrated circuit substrate; and
- Claim 8 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit structure that includes an epitaxial silicon layer that extends from an active region of an integrated circuit substrate through an insulation layer beneath the active region to an underlying substrate, wherein the epitaxial silicon layer includes a first layer in the active region in contact with a trench isolation

structure and a second layer in the active region spaced apart from the first layer.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chu et al. teach an SOI structure that features a strained silicon layer. Christensen et al., Mandelman et al., Ho et al., and Yamada et al. teach SOI structures that feature a body contact for connecting the SOI layer to an underlying semiconductor body. Lee et al. teach an SOI structure that features trench isolation structures.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813